Advanced Packaging Market Size & Share Analysis - Growth Trends and Forecast (2026 - 2031)
Industry: Semiconductors & Hardware
URL: https://www.mordorintelligence.com/industry-reports/advanced-packaging-market

Advanced Packaging Market Size and ShareMarket Overview

Study Period	2020 - 2031
Market Size (2026)	USD 57.46 Billion
Market Size (2031)	USD 90.11 Billion
Growth Rate (2026 - 2031)	9.42 %
Fastest Growing Market	Middle East
Largest Market	Asia-Pacific
Market Concentration	Medium
Major Players	*Disclaimer: Major Players sorted in no particular order

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Advanced Packaging Market Analysis by Mordor IntelligenceThe advanced packaging market size is expected to grow from USD 51.62 billion in 2025 to USD 57.46 billion in 2026 and is forecast to reach USD 90.11 billion by 2031 at 9.42% CAGR over 2026-2031. Momentum is shifting from node-shrink economics to heterogeneous integration, where chiplets, interposers and stacked-die assemblies deliver power-efficient performance that conventional monolithic scaling can no longer support economically. Fan-out wafer-level and 2.5D interposer techniques are gaining importance as sovereign-AI mandates and export-control regimes encourage on-device inference architectures that minimize cross-border technology exposure. Automotive electrification is another structural driver, because silicon-carbide power modules need copper-pillar or hybrid-bond connections to survive thermal cycling far beyond the limits of legacy wire-bond assemblies. Finally, government subsidy programs across the United States, European Union and South Korea are localizing capacity and accelerating equipment purchases that otherwise would have faced multi-year payback hurdles.

Key Report Takeaways

* By packaging platform, flip-chip led with 41.37% of the advanced packaging market share in 2025, while panel-level packaging is projected to expand at a 25.58% CAGR through 2031.
* By end-user industry, consumer electronics commanded 48.77% of the advanced packaging market size in 2025; automotive and electric-vehicle applications are advancing at a 10.11% CAGR to 2031.
* By geography, Asia-Pacific accounted for 60.57% of 2025 revenue, whereas the Middle East and Africa region is the fastest, with a 9.61% CAGR forecast to 2031.
* By device architecture, 2D ICs comprised 73.71% of 2025 shipments; 3D IC designs integrating through-silicon vias are set to grow at 9.55% through 2031.
* By interconnect technology, solder bumps retained 58.92% share in 2025, yet hybrid bonding is on track for a 10.02% CAGR, driven by sub-10-micron pitch demand in AI accelerators.

Note: Market size and forecast figures in this report are generated using Mordor Intelligence’s proprietary estimation framework, updated with the latest available data and insights as of 2026.

Global Advanced Packaging Market Trends and InsightsDrivers Impact Analysis*

Driver | (~) % Impact on CAGR Forecast | Geographic Relevance | Impact Timeline |
Rising Demand for Heterogeneous Integration for AI and HPC | +2.1% | Global, with concentration in North America and Asia-Pacific | Medium term (2-4 years) |
Miniaturization of Consumer Devices Boosting WLP Adoption | +1.6% | Global, led by Asia-Pacific manufacturing hubs | Short term (≤ 2 years) |
Government Semiconductor Subsidies (CHIPS and EU Chips Acts) | +1.8% | North America and Europe, spillover to allied nations | Long term (≥ 4 years) |
EV Power-Electronics Reliability Needs | +1.5% | Global, early adoption in Europe and China | Medium term (2-4 years) |
Emerging Glass-Core Substrates Enabling Panel-Level Packaging | +1.2% | Asia-Pacific core, technology transfer to North America | Long term (≥ 4 years) |
Co-Packaged Optics Demand in Hyperscale Data Centers | +1.3% | North America and Europe hyperscale clusters | Medium term (2-4 years) |
Source: Mordor Intelligence |

Rising Demand for Heterogeneous Integration for AI and HPC

Chiplet architectures now partition logic, memory and I/O across multiple tiles connected by high-bandwidth interposers, enabling compute density that monolithic designs cannot reach within power limits.[1]Taiwan Semiconductor Manufacturing Company, “3D IC and Advanced Packaging,” tsmc.com TSMC shipped more than 15 000 CoWoS wafers in 2025 for NVIDIA’s Hopper and Blackwell GPUs, highlighting commercial readiness. Intel’s Foveros Direct hybrid-bond technology achieves sub-10-micron pitch, cutting cache-to-core latency below 5 ns.[2]Intel Corporation, “Intel Unveils Foveros Direct 3D Packaging Technology,” intel.com Mix-and-match logic, analog and RF tiles fabricated on different nodes optimize cost and time-to-market. The trend sustains double-digit expansion in 2.5D and 3D platforms that underpin data-center accelerators and sovereign-AI initiatives.

Miniaturization of Consumer Devices Boosting WLP Adoption

Smartphones and wearables target sub-6 mm Z-heights, leaving no room for substrate-based packages. Fan-out wafer-level technology redistributes I/O across the die surface, achieving package thickness below 0.4 mm. Apple and Qualcomm have already migrated high-volume processors to fan-out, and mid-tier Android brands follow as tooling costs amortize. Wearable biosensors are adopting fan-in chip-scale packages that eliminate wire bonds, enhancing shock resistance and hermeticity. As brands prioritize thinness and battery life, the advanced packaging market gains incremental wafer-level volume across consumer segments.

Government Semiconductor Subsidies (CHIPS and EU Chips Acts)

The United States CHIPS and Science Act dedicates USD 39 billion in direct grants plus USD 75 billion in loan guarantees, explicitly naming advanced packaging as a strategic capability. TSMC’s Arizona site, backed by USD 6.6 billion in grants, will start CoWoS production in 2025. The EU Chips Act channels EUR 43 billion (USD 49.6 billion) into regional pilot lines such as Fraunhofer’s panel-level facility in Dresden. South Korea’s KRW 26 trillion (USD 0.019 trillion) package expands Samsung’s Pyeongtaek capacity by 40%. Subsidy competition is redrawing supply chains and fragmenting the advanced packaging market into regional clusters.

EV Power-Electronics Reliability Needs

Silicon-carbide MOSFET inverters face thermal cycles above 200 °C, forcing a move from wire bonds to copper-pillar and hybrid-bond connections that survive 15-year vehicle lifetimes. Infineon’s CoolSiC modules recorded zero field failures across 500 000 vehicles in 2024, validating advanced packaging for automotive power stages.[3]Infineon Technologies, “CoolSiC MOSFET,” infineon.com Tesla’s hybrid-bonded SiC modules cut parasitic inductance 30% and achieved 98.5% inverter efficiency. Automated optical inspection and X-ray laminography raise capex yet sh

rink warranty reserves, making reliability-centric packaging a core differentiator as battery costs decline.

Restraints Impact Analysis*

Restraint | (~) % Impact on CAGR Forecast | Geographic Relevance | Impact Timeline |
High Capital Intensity of Advanced Packaging Lines | -1.4% | Global, most acute in North America and Europe | Short term (≤ 2 years) |
Industry Consolidation Squeezing Outsourced Margins | -1.1% | Asia-Pacific OSAT hubs, spillover globally | Medium term (2-4 years) |
BT-Resin Substrate Capacity Bottlenecks | -0.9% | Global, supply concentrated in Japan and Taiwan | Short term (≤ 2 years) |
Shortage of Advanced Assembly Talent | -0.8% | North America and Europe, emerging in China | Long term (≥ 4 years) |
Source: Mordor Intelligence |
High Capital Intensity of Advanced Packaging Lines

Panel-level factories demand more than USD 500 million per line for lithography, electroplating and test equipment, stretching payback beyond five years at today’s utilizations. Hybrid-bonding tools priced above USD 15 million process only 30 wafers per hour, creating throughput pinch points. Depreciation cycles compress to three years because generations turn quickly, pushing operating margins for many OSATs below 15%. Government subsidies cover only 30–40% of project cost in high-wage regions, forcing private investors to bridge large funding gaps and delaying greenfield expansion.

Industry Consolidation Squeezing Outsourced Margins

Integrated device manufacturers internalize packaging to guard chiplet interconnect IP, reducing third-party volume by double digits in 2025. Samsung bundles I-Cube packaging with foundry wafers, locking customers into single-vendor ecosystems. Amkor and ASE now compete on yield and lead time rather than price alone, yet shrinking customer pools compress negotiating latitude. Smaller OSATs struggle to fund next-generation lines, risking a drop in the number of viable suppliers below 10 by 2028, which could dampen innovation and elevate supply-chain risk.

*Our forecasts treat driver/restraint impacts as directional, not additive. The impact forecasts reflect baseline growth, mix effects, and variable interactions.

Segment AnalysisBy Packaging Platform: Panel-Level Momentum Builds

Panel-level packaging accounted for a modest share in 2025, yet its segment within the advanced packaging market size is projected to expand at a 25.58% CAGR between 2026 and 2031. Flip-chip remained the volume leader with 41.37% of advanced packaging market share in the base year, but its solder-bump pitch cannot drop below 20 µm economically, limiting its future in AI accelerators. Fan-out wafer-level packages thrive in smartphones and wearables, while fan-in WLP supports cost-sensitive RF modules. Embedded-die in PCB laminates attracts automotive radar designers seeking vibration tolerance that offsets a 20% price premium.

The advanced packaging market increasingly views panel-level formats as a route to 40% lower die-handling cost by scaling to 750-mm-square glass substrates whose thermal expansion matches silicon. Equipment maturity remains a gating factor because laser-via drilling, vacuum lamination and large-field step-and-repeat lithography have yet to hit target yields. Commercial readiness is expected after 2027, so supply chains are lining up long-lead tooling orders today. Early adopters focus on data-center processors and AI accelerators where the cost penalty of yield learning curves is amortized over high average selling prices. Until pan

el platforms scale, flip-chip will keep dominating graphics processors and ASICs albeit with incremental copper-pillar refinements.

Image © Mordor Intelligence. Reuse requires attribution under CC BY 4.0. By End-User Industry: Automotive and EV Surpass Consumer Electronics

Consumer electronics captured 48.77% of the advanced packaging market size in 2025, yet its unit growth is flattening as smartphone refresh cycles lengthen. Automotive and EV applications are forecast to register a 10.11% CAGR through 2031, the fastest across all industries, reflecting the shift to 800-volt powertrains that rely on silicon-carbide modules packaged with copper pillars and hybrid bonds. Data-center and HPC demand remains robust, fueled by AI inference workloads that exploit chiplet-based GPUs and co-packaged optics.

As battery costs fall and governments impose zero-emission mandates, semiconductor content per vehicle is rising from 5% to 15% of bill-of-materials value, most of which involves advanced packages handling high voltages and harsh thermal cycles. Industrial IoT modules integrate sensors, microcontrollers and radios in system-in-package formats optimized for sub-1 W power envelopes. Healthcare wearables add hermetic fan-in WLP to satisfy biocompatibility. Aerospace and defense, while small, command premium pricing for radiation-hardened, gold-wire packages. The automotive surge ensures that the advanced packaging industry reallocates capex toward power module lines certified under IATF 16949 and ISO 26262.

By Device Architecture: 3D IC Adoption Accelerates

Within the advanced packaging market, 2D ICs still delivered 73.71% of 2025 unit shipments, yet 3D IC designs are projected to grow at 9.55% CAGR to 2031. High-bandwidth-memory stacks bonded atop logic die shrink DRAM latency 70%, enabling real-time inference for large-language models. Intel’s Foveros Direct copper-to-copper hybrid bonding drives 5 ns cache latency and removes solder layers, cutting interface power 15%.

2.5D interposers in GPUs and AI accelerators remain an intermediate architecture because their lateral placement eases thermal management while preserving short paths. Cost-sensitive analog, MCU and RF devices stay on 2D nodes where yields are mature and packaging complexity low. As electronic-design-automation tools mature for multi-die floor-planning and thermal co-simulation, more CPU vendors will disaggregate monolithic dies into chiplets, propelling 3D IC share gains. Ultimately, the balance between yield risk, thermal stacking limits and design-flow availability will dictate the migration tempo across consumer and enterprise segments.

Image © Mordor Intelligence. Reuse requires attribution under CC BY 4.0. By Interconnect Technology: Hybrid Bonding Challenges Solder Dominance

Solder bumps accounted for 58.92% of 2025 interconnect revenue, but hybrid bonding is forecast to expand at 10.02% through 2031, eroding solder’s lead in the advanced packaging market. Copper-to-copper hybrid bonds enable less than or equal to 5 µm pitch and reduce resistance 40%, which translates to double-digit power savings in AI accelerators. Solder bumps continue in cost-driven consumer devices where 40 µm pitch suffices, and mechanical compliance is valuable.

Copper pillars, once the main fine-pitch solution for smartphones, bottom out at 20 µm and now serve mid-tier use cases. Oxide-fusion direct bonding, demonstrated by Sony, achieved a 2 µm pitch for stacked CMOS image sensors and hints at future micro-bump-less paths. Each technology now targets distinct performance-cost windows, but as AI inference migrates into broader markets, the industry is converging on hybrid bonding as the default interconnect for logic-to-memory and chiplet networks that demand ultrafine pitch and minimal power loss.

Geography Analysis

Asia-Pacific contributed 60.57% of the advanced packaging market in 2025, reflecting deep clusters of foundries, outsourced assembly and test sites, and substrate makers located in Taiwan, China, South Korea and Malaysia. The region's dominance is anchored by Taiwan Semiconductor Manufacturing Company's CoWoS and Samsung's I-Cube ramps, both of which expanded monthly capacity during 2025 to satisfy AI-accelerator demand. China's Semiconductor Manufacturing International Corporation and Jiangsu Changjiang Electronics Technology added fan-out wafer-level lines for domestic smartphone and automotive customers, even though export-control limits on extreme-ultraviolet lithography curb their competitiveness at the leading nodes. Japan's substrate ecosystem, led by Ajinomoto and Ibiden, sustains a resilient material supply chain that underpins the advanced packaging market size for flip-chip and 2.5D modules.

North America is regaining share as the CHIPS and Science Act channels USD 39 billion in grants and USD 75 billion in loan guarantees toward on-shore capacity, explicitly including advanced packaging market infrastructure. TSMC's Arizona campus begins CoWoS production in 2025, while Intel expands Foveros 3D-packaging lines in New Mexico and Oregon. Amkor's USD 2 billion Arizona plant focuses on automotive silicon-carbide power modules and aerospace-qualified packages. Canada and Mexico remain limited to back-end test and low-complexity assembly. The advanced packaging market size tied to domestic-content mandates is therefore growing steadily across the continent.

Europe captured modest value in 2025, concentrated in Germany's Fraunhofer panel-level pilot line and STMicroelectronics assembly in Italy, yet the EU Chips Act's EUR 43 billion stimulus is set to double regional semiconductor share by 2030. The Middle East and Africa held a small base but is forecast to rise at 9.61% CAGR to 2031 as the United Arab Emirates and Saudi Arabia use sovereign-wealth funds to fund green-field fabs and packaging plants. South America stays limited to test and legacy assembly, with Brazil's Ceitec serving local automotive suppliers. Overall geographic dispersion reflects customer imperatives to derisk over-reliance on Taiwan, driving the advanced packaging market toward multi-regional redundancy and making site location a competitive differentiator.

Regulatory Landscape

Government industrial-policy frameworks are increasingly tying incentives and procurement to domestic advanced packaging capability. In the United States, the CHIPS and Science Act implementation has moved beyond strategy statements into named programs, including the National Advanced Packaging Manufacturing Program (NAPMP) administered through NIST, and the January 2025 CHIPS final awards that included USD 1.1 billion for the Natcast Advanced Packaging Piloting Facility (PPF) in Tempe, Arizona. In Europe, EU-level policy momentum continued with the European Commission publishing a June 2026 Chips Act 2.0 proposal that places explicit emphasis on strengthening back-end 3D advanced packaging and heterogeneous integration capabilities, reinforcing the role of regional pilot lines and coordinated funding instruments.

Standards and sustainability compliance are also tightening as capacity is localized. SEMI E177:2026 took effect in May 2026, introducing carbon footprint declaration requirements (with verification via ISO/IEC 17025 accredited laboratories) that affect export-facing 2.5D/3D chiplet packaging supply chains. This adds a formal documentation layer for advanced packaging shipments, pushing material suppliers, OSATs, and integrated device manufacturers to integrate traceability and emissions accounting into qualification processes alongside electrical and re

liability testing.

Value Chain Analysis

The advanced packaging value chain begins with upstream materials, including substrates such as BT resin and ABF-related supply, copper and chemicals, underfill, and emerging glass-core formats. It then runs through equipment, including lithography, plating, bonding, metrology, and test, and into high-precision manufacturing spanning foundry-led advanced packaging and OSAT assembly and test, before ending with downstream integration into end products across consumer devices, data-center and HPC accelerators, and automotive power electronics.

Value capture is increasingly shaped by integrated platform offerings from large foundries and IDMs, including TSMC CoWoS and Intel Foveros, while OSATs such as ASE, Amkor, and Powertech compete on yield learning, cycle time, and co-design engagement for fan-out, SiP, and heterogeneous integration programs. Bottlenecks remain concentrated in high-end 2.5D/3D capacity and in enabling inputs, and they affect how value is captured across the chain. Industry commentary in 2026 also pointed to continued tightness in 2.5D packaging capacity amid AI-driven demand, reinforcing the importance of long-term capacity reservations and multi-sourcing across ASE, SPIL, and Powertech-type partners. TSMC’s 2026 scale-up across packaging facilities in Chiayi Science Park into mass production, alongside further site expansion, underscores how packaging capacity is being built via dedicated packaging campuses. As package power density rises, thermal-management materials and architectures are becoming higher-value steps in the chain, shifting differentiation toward materials innovation and advanced inspection and test rather than cost alone.

Competitive Landscape

Market structure is moderately consolidated, the top five vendors—Taiwan Semiconductor Manufacturing Company, Samsung Electronics, Amkor Technology, ASE Technology and Intel—commanded roughly 55% revenue in 2025, yet more than 20 additional companies remain active, preserving buyer flexibility. Each leading player bundles wafer fabrication with high-density interposer, fan-out or hybrid-bond capacity, capturing a premium for turnkey service that rivals cannot easily match. Samsung integrates I-Cube packaging with foundry wafers, locking customers into a single-vendor path that shields chiplet intellectual property and secures share in the advanced packaging market size.

Outsourced assembly and test providers face margin compression as integrated device manufacturers insource heterogeneous-integration lines. Amkor answers through geographic reach—Arizona for automotive, Portugal for aerospace—and by co-design partnerships that shorten time-to-yield for fabless designers. ASE Technology pairs its Siliconware joint venture with substrate expertise to guarantee supply during BT-resin shortages, a strategy that attracts graphics-processor clients hurt by 2024 material bottlenecks. Powertech Technology and JCET Group occupy specialist niches: automotive-qualified flip-chip for Powertech and fan-out panel-level modules for JCET, both contributing incremental advanced packaging market share while avoiding head-to-head combat with top-tier rivals.

Technology remains the core battlefront. TSMC owns more than 1 200 CoWoS patents, Intel leads copper-to-copper hybrid bonding, and Applied Materials dominates in glass-substrate equipment capable of 2 µm line-and-space resolutions. Start-ups focus on software: Ansys and Cadence extend electronic-design-automation flows that co-optimize multi-die power networks and thermal paths, lowering entry barriers for niche hardware innovators. Competitive intensity therefore hinges on capex scale, patent walls and ecosystem alignment, all of which propel continuous

consolidation inside the advanced packaging market.

Advanced Packaging Industry Leaders* Amkor Technology, Inc.

* Taiwan Semiconductor Manufacturing Company Limited

* Advanced Semiconductor Engineering Inc.

* Intel Corporation

* JCET Group Co. Ltd

* *Disclaimer: Major Players sorted in no particular order

Market Opportunities and Future Outlook

Near-term whitespace is most visible where capacity constraints intersect with chiplet-heavy AI and HPC roadmaps, and where regionalization policies encourage new back-end clusters. The June 2026 announcement of a USD 1.1 billion investment by JCET Group for an advanced packaging and testing facility in Shanghai Lingang, targeting AI chips, is an example of supply-side expansion aligned with AI demand. In Taiwan, National Science and Technology Council statements in July 2026 described TSMC building additional advanced packaging facilities in Phase II of Chiayi Science Park, signaling continued ecosystem build-out around large-scale packaging hubs.

Memory and logic co-integration is also creating demand for advanced packaging lines that can handle higher layer counts, tighter pitch interconnects, and more stringent reliability qualification. SK hynix confirmed a USD 12.85 billion investment for its P&T7 advanced packaging plant in Cheongju, South Korea (reported in 2026), indicating that HBM-related packaging capacity is being treated as strategic infrastructure. Japan is also seeing packaging build-outs alongside photonics investment, with Tower Semiconductor announcing in July 2026 a USD 3 billion investment supported by USD 1 billion in Japanese government grants for expansion spanning silicon photonics and advanced packaging. Across these moves, opportunity concentrates on scalable 2.5D and 3D lines, higher-throughput bonding and test, and substrate and thermal solutions that reduce the risk of packaging becoming the gating item for accelerator and HBM supply.

Recent Industry Developments* June 2026: TSMC and Amkor Technology announced a 10-year agreement to provide advanced packaging and testing services in Arizona. The collaboration supports a more complete US-based wafer-to-package supply chain and strengthens local sourcing options for customers sensitive to lead-time and export-control exposure.
* December 2025: Samsung Electronics started mass production of I-Cube4, integrating multiple high-bandwidth-memory stacks around a logic die using hybrid bonding. The release pushed higher-density 2.5D/3D integration into production flows and raised competitive pressure on alternative interposer and bonding approaches in AI accelerator packaging.
* November 2024: CHIPS for America announced up to USD 300 million in NAPMP funding to accelerate the transition of advanced packaging innovations to high-volume manufacturing. The funding focus on scaling and piloting helped reduce early-stage risk for process transfer and tool qualification across US-based packaging ecosystems.

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Research Methodology Framework and Report ScopeMarket Definition and Coverage

For this study, the advanced packaging market is defined as the revenue generate d from semiconductor packaging approaches that go beyond traditional wire-bond m ethods, and that enable higher density, performance, and integration at the pack age level.

Scope exclusions: We exclude standard leadframe and basic wire-bond packaging wh en it is not combined with an advanced integration feature (such as fan-out, int erposers, or stacking).

Segmentation Overview

* By Packaging Platform* Flip-Chip
* Embedded Die
* Fan-in WLP
* Fan-out WLP
* 2.5D / 3D
* System-in-Package (SiP)
* Panel Level Packaging (PLP)

* By End-User Industry* Consumer Electronics
* Automotive and EV
* Data Center and HPC
* Industrial and IoT
* Healthcare / Med-tech
* Aerospace and Defense

* By Device Architecture* 2D IC
* 2.5D Interposer
* 3D IC (TSV / Hybrid-Bond)

* By Interconnect Technology* Solder Bump
* Copper Pillar
* Hybrid Bond
* Micro-bump-less Direct Bond

* By Geography* North America* United States
* Canada
* Mexico

* South America* Brazil
* Argentina
* Rest of South America

* Europe* Germany
* United Kingdom
* France
* Italy
* Spain
* Rest of Europe

* Asia-Pacific* China
* India

* Japan
* South Korea
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* Rest of Asia-Pacific

* Middle East* United Arab Emirates
* Saudi Arabia
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* Africa* South Africa
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Data Sources, Market Sizing, and Validation

Desk Research

Desk research was used to set the market boundaries, align terminology, and collect the most repeatable indicators that explain demand for advanced packaging. We relied on public sources such as semiconductor industry association releases, government trade statistics and customs dashboards, central bank and IMF macro series for currency and inflation context, and peer reviewed journals covering packaging and interconnect trends.

To ground the model inputs, we also reviewed company annual reports, earnings notes, and investor presentations to understand capacity moves and technology ramps, followed by reputable press coverage for the timing of major plant or product announcements. In addition, a paid subscription for company financials and intelligence and a patent database were used selectively to cross-check revenue exposure and technology activity in a consistent format. These are examples of sources we used, and this list is not exhaustive since many other public references were also reviewed for data collection, validation, and clarification.

Primary Interviews and Surveys

Primary work focused on validating which advanced packaging formats were being adopted, how quickly pricing was shifting, and what constraints were real in the supply chain. We spoke with a mix of equipment and materials ecosystem participants, packaging service providers, and device and system side stakeholders across APAC, EMEA, and the Americas, so the assumptions could be adjusted to match on-the-ground realities.

Distribution of primary research fieldwork respondents

Company type | Respondent position | Region |
Top tier: 32% | CXOs: 12% | APAC: 43% |
Mid tier: 46% | Functional/Unit leaders: 42% | EMEA: 32% |
Smaller Players: 22% | Managers: 46% | Americas: 25% |

Market-Sizing & Forecasting

Sizing started with a top-down build where semiconductor unit demand and value mix were reconstructed by linking packaging intensity to end-use signals, and then translating that demand pool into advanced packaging revenue through penetration and average selling price logic. We then checked the result using selective bottom-up approximations, such as sampled package ASPs multiplied by estimated volumes for key formats, supported by channel feedback on utilization and ramp timing.

Inputs used in the model were kept practical and traceable, including wafer starts and outsourcing trends, adoption curves for fan-out and 2.5D or 3D formats, substrate and interconnect shifts (for example copper pillar and hybrid bonding r

eadiness), and end-market demand markers from data center and automotive electronics cycles. Where a full supplier roll-up was not feasible, gaps were handled by using format-level penetration ranges agreed during interviews, and by keeping regional splits tied to published manufacturing footprints.

For forecasting, scenario analysis was applied, where the base case was built from consensus views on capacity additions, yield learning, and end-market demand, followed by conservative and aggressive variants to test sensitivity. The final forecast was accepted only after the variables moved together in a realistic way across technology and geography, and we could re-run the model if new data is released.

Data Validation & Update Cycle

Validation was done in layers, starting with arithmetic and unit-consistency checks, followed by variance tests against independent indicators like semiconductor revenue cycles, packaging capacity announcements, and regional trade signals. When a number looked out of line, we re-checked definitions first, then revisited the assumption that drove the swing, and in some cases re-contacted sources to confirm the direction of change.

Before sign-off, the model and narrative go through multi-step analyst reviews so the logic is understandable and the assumptions are not hidden in spreadsheets. The report is refreshed annually, and interim updates are triggered when material events occur, such as a major capacity shift, policy change, or a clear demand break. Right before delivery, a final pass is completed so clients receive the most current view based on the latest available public data.

Mordor Intelligence's Advanced Packaging Market Sizing Compared With Other Published Estimates

Published market sizes for advanced packaging often differ because the line between advanced and standard packaging is not drawn the same way, and because the assumed adoption pace of newer formats can vary across publishers. Gaps also come from which year is treated as the current size, plus how pricing is normalized across regions and translated into a single USD figure.

Wafer-start direction, OSAT utilization signals, and format adoption checks are the evidence points that keep Mordor Intelligence's estimate tied to a semiconductor demand pool where 2.5D and 3D and fan-out and SiP revenues are counted only when the advanced integration feature is present. Other totals can shift when broader conventional packaging is blended in, or when slower ASP change and slower penetration are assumed for hybrid bonding and high density interconnect formats.

Benchmark comparison

Source	Market Size	Gaps in Research Methodology
Mordor Intelligence	USD 57.46 B (2026)	
Global Consultancy A	USD 45.13 B (2025)	Uses a different base year and may apply a narrower packaging-type tally that does not fully reflect device-architecture mix shifts, which can reduce the value share assigned to 2.5D and 3D and fan-out ramps.
Industry Research Group B	USD 39.60 B (2024)	Anchors the current size to an earlier year and appears to apply slower penetration and price progression, which can understate revenue uplift from higher density interconnect and advanced substrate usage.

The table shows that timing and scope rules explain much of the spread, even before you get into forecasting style. Our sizing keeps each technology counted through a clear inclusion test, and the final number is cross-checked against demand and utilization signals so the steps can be repeated when the market moves.

Key Questions Answered in the ReportHow large will the advanced packaging market be by 2031? It is projected to reach USD 90.11 billion by 2031, expanding at 9.42% CAGR from 2026 to 2031.

Which region dominates revenue today? Asia-Pacific held 60.57% of 2025 revenue thanks to dense manufacturing ecosystems in Taiwan, China and South Korea.

What is the fastest-growing end-user segment? Automotive and EV applications are forecast to post a 10.11% CAGR through 2031 as silicon-carbide power modules adopt copper-pillar and hybrid bonds.

Why is hybrid bonding important? It enables less than or equal to 5 µm interconnect pitch, lowers resistance 40% and is expanding at 10.02% CAGR, displacing solder bumps in AI accelerators.

How are subsidies reshaping supply chains? U.S., EU and South Korean incentive programs tie grants to domestic content, driving new CoWoS, Foveros and panel-level lines outside traditional Asia hubs.

What limits small OSAT entrants? Capital intensity above USD 500 million per panel-level line and rapid depreciation compress margins, making financing difficult without customer prepayments.

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